UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/713,406 | 11/14/2003 | Bryan M. Cantrill | 03226.337001; SUN040164 | 7014 |

32615 7590 07/17/2006

OSHA LIANG L.L.P./SUN
1221 MCKINNEY, SUITE 2800
HOUSTON, TX 77010

| EXAMINER | |
|---|---|
| PHAM, THAI V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2194 | |

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/713,406 | CANTRILL, BRYAN M. | |
| | Examiner | Art Unit | |
| | Thai Van Pham | 2194 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This is the initial office action based on the application filed on June 20, 2006. Claims 1 - 33 are currently pending and have been considered below.

### *Claim Objections*

1. Claim 13 is objected to because of the following informalities: lack of antecedent bases. Claim 13 refers to "*the first processor*"; however, a first processor is not previously cited anywhere as an antecedence in Claim 1 – the parent claim of Claim 13 – and Claim 13. The Examiner assumes "*the first processor*" is meant to be "*a first processor*".

2. Claims 16 and 28 are objected to because of the following informalities: typo.

-- Claim 16: In the 2nd paragraph, the claim recites "*determining a second state value of the of the second speculative buffer.*" The Examiner assumes the extra "*of the*" is a typo.

-- Claim 28: In the 1st paragraph, the claim recites "*a second speculative buffer... wherein _ second speculative buffer*". The Examiner assumes the word "*the*" is missing in the 2nd recitation of the "*second speculative buffer*".

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 3, 6 – 9, 17 – 20, 23 – 26, and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by **Bunnell** (10/713,406).

-- Claim 1: **Bunnell** discloses a method of a speculative tracing (i.e., instrumentation event tracing), comprising:

• defining the speculative tracing using a plurality of probes (i.e., static and dynamic instrumentation of routines; Page 5 Lines 12 – 50);

• firing at least one of the plurality of probes defined by the speculative tracing (Page 6 Lines 14 – 38);

• if one of the plurality of probes comprises a first speculation function, allocating at least one instance of a first speculative buffer arranged to transfer data to a first principal buffer (i.e., trace control routines and trace data buffer; Fig. 4, Page 6 Lines 53 – 64, Page 7 Lines 13 – 24); and

• determining a first state value associated with the first speculative buffer (i.e., progression stages of the trace process flow Fig. 4, Page 6 Line 53 – Page 7 Line 12, Page 7 Lines 25 – 33).

-- Claim 2: **Bunnell** discloses the method of Claim 1 and further discloses the first state value comprises at least one of a group consisting of a speculate-one state, a speculate-many state, a commit-one state, a commit-many state, and a discard state (Figs. 7 – 8, Page 8 Line 60 – Page 10 Line 51).

-- Claim 3: **Bunnell** discloses the method of Claim 2 and further discloses the speculate-one state corresponds to firing one of the plurality of probes comprising a first speculate function on a first processor (i.e., operation of entry and exit trace data collection control routines; Figs. 2 – 3, Lines 14 – 37).

-- Claims 6 and 7: **Bunnell** discloses the method of Claim 2 and further discloses the commit-one state and the commit-many state correspond to firing one of the plurality of probes comprising a commit function (i.e., controlling the transferring of the collected trace data to trace data buffers; Fig. 8, Page 10 Line 50 – Page 11 Line 5).

-- Claim 8: **Bunnell** discloses the method of Claim 2 and further discloses the discard state corresponds to firing one of the plurality of probes comprising a discard function (i.e., controlling the transferring of the collected trace data to trace data buffers; Fig. 8, Page 10 Line 50 – Page 11 Line 5).

-- Claim 9: **Bunnell** discloses the method of Claim 1 and further discloses the method further comprising modifying a size of the first speculative buffer (Page 4, Lines 55 – 62).

-- Claim 17: **Bunnell** discloses a system for a speculative tracing using a tracing framework, comprising:

- a first principal buffer configured to store data from the tracing framework and associated with a first processor (i.e., start, end, and main buffers; Fig. 1, Page 4 Line 30 – Page 5 Line 4);
- a first instance of a first speculative buffer associated with the first principal buffer and configured to transfer data to the first principal buffer (i.e., system and user trace buffers; Fig. 1, Page 4 Line 30 – Page 5 Line 4), wherein the first speculative buffer has a first state value associated therewith (Figs. 7 – 8, Page 8 Line 60 – Page 10 – Line 51); and
- a plurality of probes defining the speculative tracing executing on the tracing framework; wherein the first state value is updated upon firing at least one of the plurality of probes (Page 5, Lines 15 – 50).

-- Claim 18: **Bunnell** discloses the system of Claim 17 and further discloses the first state value comprises at least one of a group consisting of an active state, a speculate-one state, a speculate-many state, a commit-one state, a commit-many state and a discard state (Figs. 7 – 8, Page 8 Line 60 – Page 10 Line 51).

-- Claim 19: **Bunnell** discloses the system of Claim 18 and further discloses the active state corresponds to firing one of the plurality of probes comprising a first speculation function (Fig. 7, Page 9, Table 2).

-- Claim 20: **Bunnell** discloses the system of Claim 18 and further discloses the speculate-one state corresponds to firing one of the plurality of probes comprising a first speculate function (i.e., operation of entry and exit trace data collection control routines; Figs. 2 – 3, Lines 14 – 37).

-- Claims 23 – 24: **Bunnell** discloses the system of Claim 18 and further discloses the commit-one state and the commit-many state correspond to firing one of the plurality of probes comprising a commit function (i.e., controlling the transferring of the collected trace data to trace data buffers; Fig. 8, Page 10 Line 50 – Page 11 Line 5).

-- Claim 25: **Bunnell** discloses the system of Claim 18 and further discloses the discard state corresponds to firing one of the plurality of probes comprising a discard function (i.e., controlling the transferring of the collected trace data to trace data buffers; Fig. 8, Page 10 Line 50 – Page 11 Line 5).

-- Claim 26: **Bunnell** discloses the system of Claim 17 and further discloses a size of the first speculative buffer is configurable (Page 4, Lines 55 – 62).

-- Claim 32: **Bunnell** discloses a computer system for a speculative tracing comprising:

- a first processor, a memory, a storage device (Fig. 1, Page 4 Line 30 – Page 5 Line 4); and
- software instructions stored in the memory for enabling the computer system to:
  - define the speculative tracing using a plurality of probes (i.e., static and dynamic instrumentation of routines; Page 5 Lines 12 – 50);
  - fire at least one of the plurality of probes defined by the speculative tracing (Page 6 Lines 14 – 38);
  - allocate at least one instance of a first speculative buffer arranged to transfer data to a first principal buffer, if one of the plurality of probes comprises a first speculation function (i.e., trace control routines and trace data buffer; Fig. 4, Page 6 Lines 53 – 64, Page 7 Lines 13 – 24); and
  - determine a first state value associated with the first speculative buffer (i.e., progression stages of the trace process flow Fig. 4, Page 6 Line 53 – Page 7 Line 12, Page 7 Lines 25 – 33).

## *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a

person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 – 5, 10 – 12, 13 – 16, 21 – 22, 27 – 31, and 33 are rejected under 35 U.S.C. 103(a) as being obvious over **Bunnell** (10/713,406).

-- Claim 4: **Bunnell** discloses the method of Claim 2 but does not explicitly disclose that the speculate-many state corresponds to firing one of the plurality of probes comprising a second speculate function on a second processor. The Applicant specifically discloses that speculative tracing can be associated with one or more processors. The Examiner notes that although The Applicant discloses that more than one processors can be used in speculative tracing, he does not specify any critical or significant advantages for using multiple processors over a single one. In a multi-processor system, different processes or sub-processes in an application could be simultaneously executed if they are independent from one another. In instrumentation of tracing events of a system having multiple processors, concurrent gathering of tracing data from independent routines is highly desirable to speed up processing time. Thus, it would have been obvious to one with ordinary skills in the art of software development at the time the invention was made, in a multi-processor system implementing **Bunnell**'s method of Claim 2, to fire one or more probes comprising a second speculate function associated with a processor other than the first one.

-- Claim 5: **Bunnell** discloses the method of Claim 1 but does not explicitly disclose that a second instance of the first speculative buffer is arranged to transfer data to a second principal buffer. The Examiner notes that although The Applicant discloses

that more than one principal buffers can be used in speculative tracing, he does not specify any critical or significant advantages for using multiple principal buffers over a single one for storing data from the respective speculative buffer(s). When a system contains more than one physical memory components accessible for data tracing, if the amount of traced data is substantially larger than the storage capacity of any single temporary or speculative memory component, it would be advantageous for the application to be capable of employing more than one instances of speculative memories and if necessary, more than one principal buffers. Thus, it would have been obvious to one with ordinary skills in the art of software development at the time the invention was made, in a multi-memory-component system implementing **Bunnell**'s method of Claim 1, to allocate a second instance of the first speculative buffer to transfer data to a second principal buffer. On a further note, although the application may employ more than one physical memory components in the implementation of speculative and/or principal buffers, the actual allocation of memory in a software process is seamless and transparent to the user as long as memory selection and the respective address ranges are properly taken care of at the firmware level.

-- Claims 10 – 12: **Bunnell** discloses the method of Claim 1 but does not explicitly disclose that the method further comprising incrementing a drop counter for a speculative drop of data in the first speculative buffer, wherein the speculative drop of data corresponds to failing to transfer the data from the first speculative buffer and/or failing to store the data in the first speculative buffer. **Bunnell**, however, further

discloses a buffer management flow for controlling the operation of trace buffers (Fig. 8, Page 10 Line 50 – Page 11 Line 5), including the encountering and handling of buffer overflow. Official Notice is taken that it is old and well known in the art of software development that in the hardware/software implementation of FIFO/LIFO (i.e., buffers), overflow and underflow events consisting of failing to store data to and failing to transfer data from FIFO/LIFO respectively, must be recorded and informed to user. Furthermore, the number of occurrences of overflow and underflow events must also be recorded; a counter is typically implemented for keeping count. The main purpose for keeping track of these erroneous events and the number of their occurrences is to keep the user informative and when necessary to provide control information for correction and/or retransmission of data. Thus, it would have been obvious to a person with ordinary skills in the art of software development at the time the invention was made to implement a drop counter for counting speculative drop of data, where the speculative drop of data corresponds to failing to transfer the data from the first speculative buffer and/or failing to store the data in the first speculative buffer.

-- Claims 13 – 15: **Bunnell** discloses the method of Claim 1 but does not explicitly disclose that the method further comprising executing a cleaning operation for each speculative buffer associated with the first processor, where the cleaning operation occurs at a specified cleaning rate and/or comprises resetting the first speculative buffer. **Bunnell**, however, further discloses that the buffer management flow controls data transfer to trace buffers by controlling their data write pointers,

including buffer empty and full conditions as well as cyclic/non-cyclic overwrite of event data (Fig. 8, Page 10 Line 52 – Page 11 Line 5). Official Notice is taken that it is old and well known in the art of software development that in the hardware/software implementation of FIFO/LIFO (i.e., buffers), flushing (i.e., cleaning) a FIFO/LIFO as well as resetting it – or rather resetting its data read and write pointers – to an empty state occurs at a maximum rate dictated by the clock frequency at which the buffer operates. Several scenarios can occur in which cleaning a trace data buffer is necessary. For example, in case of a buffer underflow/overflow condition is detected, the data accumulated in the buffer may be disregarded because the dropped data is crucial to the entire trace event as a whole. In such cases, the tracing application can configure the flushing rate or resetting of FIFO/LIFO at a rate appropriate for the application, as long as the rate is less than a maximum rate specified by the clock frequency. Thus, it would have been obvious to a person with ordinary skills in the art of software development at the time the invention was made to further add to the method of Claim 1 a step of executing a cleaning operation for each speculative buffer associated with the first processor, where the cleaning operation occurs at a specified cleaning rate and/or comprises resetting the first speculative buffer.

-- Claim 16: **Bunnell** discloses the method of Claim 1 but does not explicitly disclose that the method further comprising:

• allocating a second speculative buffer arranged to transfer data to the first principal buffer, if one of the plurality of probes comprising a second speculation

function fires on a second processor. The Applicant specifically discloses that more than one speculative buffers can be associated with one or more processors in speculative tracing. The Examiner notes that although The Applicant discloses that multiple processors can be used, he does not specify any critical or significant advantages for using multiple processors over a single one in the application under examination. Furthermore, The Applicant does not specify any critical or significant advantages for using multiple speculative buffers over a single one for storing temporary or speculative data trace events. In a multi-processor system, different processes or sub-processes in an application could be simultaneously executed if they are independent from one another. In instrumentation of tracing events of a system having multiple processors, concurrent gathering of tracing data from independent routines is highly desirable to speed up processing time. In addition, when more than one physical memory components are available for data tracing, if the amount of temporary traced data is substantially larger than the storage capacity of any single temporary or speculative memory component, it would be advantageous for the application to be capable of employing more than one instances of speculative memories. Thus, it would have been obvious to one with ordinary skills in the art of software development at the time the invention was made, in a multi-processor and multi-memory component system, to further add to **Bunnell**'s method of Claim 1 a step comprising allocating a second speculative buffer arranged to transfer data to the first principal buffer, if one of the plurality of probes comprising a second speculation function fires on a second processor; and

• determining a second state value of the second speculative buffer. Since a second probe and its associated speculation function and speculative buffer operate independently on a second processor, it would have been obvious to a person with ordinary skills in the art of software development at the time the invention was made to add to the method above a step determining a second state value of the second speculative buffer, where the second state value is similar to the first state value disclosed in **Bunnell**'s method of Claim 1(Figs. 7 – 8, Page 8 Line 60 – Page 10 Line 51).

-- Claim 21: **Bunnell** discloses the system of Claim 18 and does not explicitly disclose that the speculate-many state corresponds to firing one of the plurality of probes comprising a second speculate function on a second processor. The Applicant specifically discloses that speculative tracing in a multi-processor system is one of the several embodiments of the inventive application under examination. The Examiner notes that although The Applicant discloses that more than one processors can be used in speculative tracing, he does not specify any critical or significant advantages for using multiple processors over a single one. In a multi-processor system, different processes or sub-processes in an application could be simultaneously executed if they are independent from one another. In instrumentation of tracing events of a system having multiple processors, concurrent gathering of tracing data from independent routines is highly desirable to speed up processing time. Thus, it would have been obvious to one with ordinary skills in the art of software development at the time the invention was

made, in a multi-processor system implementing **Bunnell**'s system of Claim 18, to associate the speculate-many state with firing one of the plurality of probes comprising a second speculate on a processor other than the first one.

-- Claim 22: **Bunnell** discloses the system of Claim 21 and does not explicitly disclose that a second principal buffer configured to store data from the tracing framework and associated with the second processor, wherein a second instance of the first speculative buffer is associated with the second principal buffer and configured to transfer data to the second principal buffer. The Examiner notes that although The Applicant discloses that more than one principal buffers can be used in speculative tracing, he does not specify any critical or significant advantages for using multiple principal buffers over a single one for storing data from the respective speculative buffers. When a system contains more than one physical memory accessible for data tracing, if the amount of traced data is substantially larger than the storage capacity of any single temporary or speculative memory component, it would be advantageous for the application to be capable of employing more than one instances of speculative memories and if necessary, more than one principal buffers. Thus, it would have been obvious to one with ordinary skills in the art of software development at the time the invention was made, in a multi-processor and multi-memory-component system implementing **Bunnell**'s system of Claim 21, to use a second principal buffer in association with the second speculative buffer running on a second processor. On a further note, although the application may employ more than one physical memory

components in the implementation of speculative and/or principal buffers, the actual allocation of memory in a software process is seamless and transparent to the user as long as memory selection and the respective address ranges are properly taken care of at the firmware level.

-- Claim 27: **Bunnell** discloses the system of Claim 17 but does not explicitly disclose that the system further comprising a drop counter for a speculative drop of data in the first speculative buffer. **Bunnell**, however, further discloses a buffer management flow for controlling the operation of trace buffers (Fig. 8, Page 10 Line 50 – Page 11 Line 5), including the encountering and handling of buffer overflow. Official Notice is taken that it is old and well known in the art of software development that in the hardware/software implementation of FIFO/LIFO (i.e., buffers), overflow and underflow events consisting of failing to store data to and failing to transfer data from FIFO/LIFO respectively, must be recorded and informed to user. Furthermore, the number of overflow and underflow events must also be recorded; a counter is typically used for counting. The main purpose for keeping track of these erroneous events and the number occurrences is to keep the user informative and when necessary to provide data information for correction and/or retransmission of data. Thus, it would have been obvious to a person with ordinary skills in the art of software development at the time the invention was made to further implement a drop counter for counting speculative drop of data in the **Bunnell**'s system of Claim 17..

-- Claim 28: **Bunnell** discloses the system of Claim 17 but does not explicitly disclose that the system further comprising:

• a second speculative buffer associated with the first principal buffer and configured to store data and transfer data to the first principal buffer. The Examiner notes that although The Applicant discloses that more than speculative buffers can be used in speculative tracing, he does not specify any critical or significant advantages for using multiple speculative buffers over a single one. When a system contains more than one physical memory components accessible for data tracing, if the amount of traced data is substantially larger than the storage capacity of any single temporary or speculative memory component, it would be advantageous for the application to be capable of employing more than one instances of speculative memories. Thus, it would have been obvious to one with ordinary skills in the art of software development at the time the invention was made, in a multi-processor and multi-memory-component system implementing **Bunnell**'s system of Claim 17, to use a second principal buffer in association with the second speculative buffer running on a second processor. On a further note, although the application may employ more than one physical memory components in the implementation of speculative and/or principal buffers, the actual allocation of memory in a software process is seamless and transparent to the user as long as memory selection and the respective address ranges are properly taken care of at the firmware level;

• the second speculative buffer has a second state value associated therewith; and the second state value is updated upon firing at least one of the plurality of probes.

Since the second speculative buffer is operated independently from the first speculative buffer, it would have been obvious to a person with ordinary skills in the art of software development at the time the invention was made to add to the system above a second state value associated with the second speculative buffer, where the second state value is similar to the first state value which is updated upon firing it associated probe(s) (Figs. 7 – 8, Page 8 Line 60 – Page 10 Line 51).

-- Claim 29: **Bunnell** discloses the system of Claim 28 but does not explicitly disclose that the first instance of the first speculative buffer and second speculative buffer are located in respective cells of an array. Official Notice is taken that it is old and well known in the art of software development that the buffering of data is conventionally accomplished by implementation of array or similarly, allocation of data memory pointers, which ultimately lead to the storage of information on a physical – and usually contiguous – block of memory cells on a physical memory. An array is a software data structure that provides the user with the ability to allocate a chunk of physical memory for storing data; therefore, an array can be segmented into sub-blocks of cells where each corresponds to a dedicated "buffer". Thus, it would have been obvious to a person with ordinary skills in the art of software development at the time the invention was made locate the first instance of the first speculative buffer and second speculative buffer in respective cells of an array in **Bunnell**'s system of Claim 28.

-- Claim 30: **Bunnell** discloses the system of Claim 28 but does not explicitly disclose that the second state value comprises at least one of a group consisting of an active, a speculate-one state, speculate-many state, commit state, and commit-many state, and a discard state. **Bunnell**, however, discloses the first state of the system of Claim 17 comprises at least one of a group consisting of an active state, a speculate-one state, a speculate-many state, a commit-one state, a commit-many state and a discard state (Figs. 7 – 8, Page 8 Line 60 – Page 10 Line 51). The second state is simply another instance of a state having the same group value as the first state but associated with a second speculative buffer. Thus, it would have been obvious to a person with ordinary skills in the art of software development at the time the invention was made to assign the second state value of **Bunnell**'s system in Claim 28 to at least one of a group consisting of an active, a speculate-one state, speculate-many state, commit state, and commit-many state, and a discard state.

-- Claim 31: **Bunnell** discloses the system of Claim 30 and but does not explicitly disclose that the active state corresponds to firing one of the plurality of probes comprising a second speculation function. **Bunnell**, however, discloses the active state of the system of Claim 18 corresponds to firing one of the plurality of probes comprising a first speculation function (Fig. 7, Page 9, Table 2). Since the second speculation function is independent from but simply another instantiation of the first speculation function, it would have been obvious to a person with ordinary skills in the art of software development at the time the invention was made to recognize that the active

state of Claim 30 corresponds to firing one of the plurality of probes comprising a second speculation function.

-- Claim 33: **Bunnell** discloses the system of Claim 32 but does not explicitly further disclose that the system further comprising software instructions stored in the memory for enabling the computer system to:

• allocate a second speculative buffer arranged to transfer data to the first principal buffer, if one of the plurality of probes comprising a second speculation function fires on the first processor. The Applicant specifically discloses that more than one speculative buffers can be associated with one or more processors in speculative tracing. The Examiner notes that The Applicant does not specify any critical or significant advantages for using multiple speculative buffers over a single one for storing temporary or speculative data trace events. When more than one physical memory components are available for data tracing, if the amount of temporary traced data is substantially larger than the storage capacity of any single temporary or speculative memory component, it would be advantageous for the application to be capable of employing more than one instances of speculative memories. Thus, it would have been obvious to one with ordinary skills in the art of software development at the time the invention was made, in multi-memory component system, to further add to **Bunnell**'s system of Claim 32 software instructions comprising allocating a second speculative buffer arranged to transfer data to the first principal buffer, if one of the plurality of probes comprising a second speculation function fires on the first processor; and

• determine a second state value of the second speculative buffer. Since the first and second speculative buffers operate independently from one another, it would have been obvious to a person with ordinary skills in the art of software development at the time the invention was made to add to the system above software instructions determining a second state value of the second speculative buffer, where the second state value is similar to the first state value which is updated upon firing it associated probe(s) (Figs. 7 – 8, Page 8 Line 60 – Page 10 Line 51)

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

• **Yamashita** (6,467,083): a debugging system for computer program, method for checking target program and information storage medium for storing checking program. Yamashita discloses a technique to select pieces of trace data information to be stored in temporary data buffer and subsequently, persistent data storage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Van Pham whose telephone number is (571) 270-1064. The examiner can normally be reached on Monday - Thursday, 9am - 5pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Myhre can be reached on (571) 270-1065. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TVP

TVP

James Myhre
Supervisory Patent Examiner